

Examiner kyoung Lee /inventor Date Considered 10/27/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

U.S. Department of Commerce, Patent and Trademark Office		Atty. Docket No.	Serial No.
		M-15302-1P US	10/798,540
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>O I P E</i> <i>SEARCHED</i> <i>AUG 10 2005</i> <i>PATENT & TRADEMARK OFFICE</i>		Applicant(s)	
(Use several sheets if necessary)		Savastiouk et al.	
		Filing Date	Group
		March 10, 2004	Unassigned

U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
KL	AA	5,391,514	Feb. 1995	Gall et al.			
KL	AB	6,903,443	Jun. 2005	Farnsworth et al.			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						

Foreign Patent Documents							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
<i>-----</i>							<i>-----</i>	<i>-----</i>

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
<i>-----</i>	<i>-----</i>	<i>-----</i>					
<i>-----</i>	<i>-----</i>	<i>-----</i>					
<i>-----</i>	<i>-----</i>	<i>-----</i>					
<i>-----</i>	<i>-----</i>	<i>-----</i>					
<i>-----</i>	<i>-----</i>	<i>-----</i>					
<i>-----</i>	<i>-----</i>	<i>-----</i>					
<i>-----</i>	<i>-----</i>	<i>-----</i>					
<i>-----</i>	<i>-----</i>	<i>-----</i>					

Examiner Kyoung Lee hyungsae Date Considered 10/27/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

U.S. Department of Commerce, Patent and Trademark Office		Atty. Docket No.	Serial No.
		M-15302-1P US	10/798,540
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Applicant(s)	
(Use several sheets if necessary)		Savastiouk et al.	
		Filing Date	Group
		March 10, 2004	2812

U.S. Patent Applications

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
KL	AA	2002/0048916	25 Apr. 2002	Yanagida			
KL	AB	6,175,158	16 Jan. 2001	Degani et al.			
KL	AC	2003/0080437	1 May 2003	Gonzalez et al.			
KL	AD	6,661,088	9 Dec. 2003	Yoda et al.			
KL	AE	2002/0036340	28 Mar. 2002	Matsuo et al.			
KL	AF	2003/0047798	13 Mar. 2003	Halahan			
KL	AG	2002/0074637	20 Jun. 2002	McFarland			
KL	AH	2002/0175421	28 Nov. 2002	Kimura			
KL	AI	2003/0116859	26 Jun. 2003	Hashimoto			
KL	AJ	6,322,903	27 Nov. 2001	Siniaguine et al.			

Foreign Patent Documents

						Translation		
		Document	Date	Country	Class	Subclass	Yes	No
KL	AK	195 31 158 A1	27 Feb. 1997	DE			X	
KL	AL	08-236579	13 Sept. 1996	JP			X	
KL	AM	0 193 128	3 Sept. 1986	EP			X	

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AN	"Solving Soldering Hierarchy Problems by Metallurgy and Design" IBM Technical Disclosure Bulletin, IBM Corp. New York, US, vol. 33, no. 8, January 1991, pages 298-299, XP000106967, ISSN: 0018-8689

Examiner Kyoung Lee Date Considered 10/27/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

U.S. Department of Commerce, Patent and Trademark Office				Atty. Docket No.	Serial No.			
				M-15302-1P US	10/798,540			
O T R INFORMATION DISCLOSURE STATEMENT BY APPLICANT MAR 29 2004 PATERSON, NJ 07054-2300				Applicant(s)				
(Use several sheets if necessary)				Savastiouk et al.				
				Filing Date	Group			
				March 10, 2004	Unassigned			
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
KL	AA	2003/0047798A1	13 Mar 2003	Halahan				
KL	AB	2003/0226254A1	11 Dec. 2003	Koning et al.				
KL	AC	2003/0211720A1	13 Nov. 2003	Huang et al.				
KL	AD	6,498,074	24 Dec. 2002	Siniaguine et al.				
KL	AE	6,498,381	24 Dec. 2002	Halahan et al.				
KL	AF	6,322,903	27 Nov. 2001	Siniaguine et al.				
KL	AG	6,163,456	19 Dec. 2000	Suzuki et al.				
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
KL	AH	WO 01/45476 A1	21 Jun. 2001	PCT				
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
KL	AI	Perfecto, Eric; Lee, Kang-Wook; Hamel, Harvey; Wassick, Thomas; Cline, Christopher; Oonk, Matthew; Feger, Claudio; McHerron, Dale, "Evaluation of Cu Capping Alternatives for Polymide-Cu MCM-D" IEEE, 2001 Electronic Components and Technology Conference.						
KL	AJ	Pang, John H.L.; Chong, D.Y.R.; Low T.H. "Thermal Cycling Analysis of Flip-Chip Solder Joint Reliability" IEEE Transactions on Components and Packaging Technologies, Vol. 24, No. 4, Dec. 2001, pages 705-712.						
KL	AK	Painaik, Mandar; and Hurley, Jim "Process Recommendations for Assembly of Flip Chips Using No-Flow Underfill" Semiconductor Products, Technical Bulletin, www.cooksonsemi.com .						
KL	AL	Ekstrom; Bjorn "Thin Film Silicon Substrates For Lead Frame Packages" Advancing Microelectronics - May/June 2003, pages 6-7.						
KL	AM	Gilleo, Ken "Substrates for Flip Chips" "Flip Chips Technology" in Area Array Packaging Handbook - Manufacturing and Assembly; K Gillio, Editor; The McGraw-Hill Companies, Inc., New York, NY.						
KL	AN	Maiwald, Werner "Soldering SMD's Without Solder Paste" http://www.midwestpcb.com/sales/Kehoe/maiwald.htm .						
KL	AO	Staychip; 2078E No-Flow Fluxing Underfill; For Soldering Sn/Pb eutectic solder bumps to common pad metallizations Preliminary Technical Bulletin" Semiconductor Products, Technical Bulletin; Cookson Electronics.						
Examiner <u>Kyang Lee</u>			Date Considered <u>10/27/05</u>					
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.								

U.S. Department of Commerce, Patent and Trademark Office		Atty. Docket No.	Serial No.
		M-15302-1P US	10/798,540
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Applicant(s)	
(Use several sheets if necessary)		Savastiouk et al.	
		Filing Date	Group
		March 10, 2004	Unassigned
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)			
KL	AP	"Design Notes: Understanding Ball Grid Array Packages" Electronics by Design, www.electronicsbydesign.com.au , issue 1997.10, pages 1-4.	
KL	AQ	Sperling, Ed; Electronic News, 9/17/2003.	
KL	AR	"Introduction to Printed Wiring Boards" Netpack Education Pool, page 1-18.	
KL	AS	"Production Qualification Report: Select Qual B: Strand Substrate on MCM MQFP Qual" Amkor Technology, Date Released: June 14, 2002.	
KL	AT	"Strand is Closing the Enterprise" Strand Interconnect AB, Viggengatan5, SE-602 09 Norrkoping Sweden, www.strandinter.se .	
KL	AU	"200mm Wafer Fab" Strand Interconnect, Partner for High Performance Electronics.	
KL	AV	Guenin, Bruce M. "The Many Flavors of Ball Grid Array Packages" Electronics Cooling, Feb. 2002, pages 1-7.	
KL	AW	"HPMX-5001: Demonstration Circuit Board: Application Brief 102" Hewlett Packard, pages 1-10.	
KL	AX	Moon, K.W.; Boettigner, W.J.; Kattner, U.R.; Biancaniello, F.S.; Handwerker, C.A. "The Ternary Eutectic of Sn-Ag-Cu Colder Alloys" Metallurgy Division, Materials Science and Engineering Laboratory NIST Gaithersburg, MD 20899 USA.	
KL	AY	Lu, H. and Bailey, C. "Predicting Optimal Process Conditions for Flip-Chip Assembly Using Copper Column Bumped Dies" School of Computing and Mathematical Sciences, 2002 IEEE, 2002 Electronics Packaging Technology Conference, pages 338-343.	
KL	AZ	Wang, Tie; Tung, Francisca; Foo, Louis; and Dutta, Vivek "Studies on A Novel Flip-Chip Interconnect Structure – Pillar Bump" Advanpack Solutions Pte Ltd, 2001 IEEE, 2001 Electronic Components and Technology Conference.	
KL	BA	United States Patent Application No. 10/739,707, entitled "Packaging Substrates For Integrated Circuits and Soldering Methods," Filed on December 17, 2003; Attorney Docket No.: M-15278 US.	
KL	BB	"Technical Data Sheet: No-Clean Pin-Probe Testable Solder Paste: NC253" www.aimsolder.com .	
KL	BC	Zama, Satoru; Baldwin, Daniel F; Hikami, Toshiya; Murata, Hideaki "Flip Chip Interconnect Systems Using Wire Stud Bumps and Lead Free Solder," 2000 IEEE Electronic Components and Technology Conference, pages 1111-1117.	
Examiner <u>Kyoung Lee</u> <u>kyounglee</u>		Date Considered <u>10/27/05</u>	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.			

U.S. Department of Commerce, Patent and Trademark Office		Atty. Docket No.	Serial No.
		M-15302-1P US	10/798,540
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Applicant(s)	
(Use several sheets if necessary)		Savastiouk et al.	
		Filing Date	Group
		March 10, 2004	Unassigned
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)			
KL	BD	Wang, C.H.; Holmes, A.S.; Gao, S. "Laser-Assisted Bump Transfer for Flip Chip Assembly," 2000 IEEE Int'l Symp on Electronic Materials & Packaging, pages 86-90.	
KL	BE	Gekhtin, Vadim; Bar-Cohen, Avram; Witzman, Sorin "Coffin-Mason Based Fatigue Analysis of Underfilled DCAs," 1998 IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A, Volume 21, No. 4, December 1998, pages 577-584.	
KL	BF	Tran, S.K.; Questad, D.L.; Sammakia, B.G. "Adhesion Issues in Flip-Chip on Organic Modules," 1998 InterSociety Conference on Thermal Phenomena, pages 263-268.	
KL	BG	"Chapter 7: Wedge and Double Cantilever Beam Tests on a High Temperature Melt Processable Polyimide Adhesive, TPER-BPDA-PA," pages 221-242.	
KL	BH	"Flip Chip Bonding in Practice" Issue No. 7, September 2001, The Micro Circuit Engineering Newsletter.	
KL	BI	www.flipchips.com/tutorial27.html "Flipchips: Tutorial 27, Shaping Gold Stud Bumps" Pages 1-8.	
KL	BJ	Jordan, Jerry "Gold Stud Bump In Flip-Chip Applications," 2002 Palomar Technologies, Inc.	
	BK	Jasper, Jorg "Gold or Solder Chip Bumping, the choice is application dependent" Chip Interconnection, EM Marin, pages 1-4.	
<p>Examiner <u>Kyoungh Lee</u> Date Considered <u>10/27/05</u></p> <p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.</p>			